IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

On page 1, please add the following heading before the first paragraph:

--Claim of Priority under 35 U.S.C. §119--

On page 2, please replace paragraph [1007] with the following amended paragraph:

There is, therefore, a need in the art for techniques to provide proper sample timing for receive diversity and/or high SINR operating environments.

On page 15, please replace paragraph [1067] with the following amended paragraph:

In a third diversity DLL scheme, one DLL is maintained for each signal instance being processed, and each DLL is operated to track the individual timing of the assigned signal instance. This may be achieved by operating one loop filter for each signal instance, with each loop filter being operated independently and updated based solely on the error metric derived for its assigned signal instance. This DLL scheme may be implemented using the pilot processor design shown in FIG. 4A whereby one loop filter 430 is included in each pilot processor 410 and is used to track the timing of the assigned signal instance. However, the register(s) within each loop filter are not loaded with the loop filter value from another loop filter, as [[is]] <u>in</u> the case for the first DLL scheme.

On page 18, please replace paragraph [1079] with the following amended paragraph:

Within each slave pilot processor 412, interpolator 420 resamples the ADC samples based on the modified time offset, $t_{adj,s}$. Despread I & D element 422 then (1) despreads the interpolated samples with the PN sequence (the same PN sequence is provided to the master and slave pilot processors assigned to process a given signal instance), (2) accumulates the despread samples over each pilot burst, and (3) provides a pilot sample for the pilot burst based on the

interpolated samples at the modified time offset. The pilot samples from despread I & D element 422 are then filtered by pilot filter 436 to provide a filtered pilot for the modified time offset. The filtered pilots from slave pilot processors 412a and 414b are provided to controller 440 and may further be processed to provide an estimate of the pilot SINRs for the modified time offsets of $t_{adj,s1}$ and $t_{adj,s2}$. Slave pilot processors 412a and 412b are thus used to determine the pilot SINRs at ± 1 chipx8 unit from the time offset, t_{adj}, determined by the master pilot processor.

On page 18, please replace paragraph [1080] with the following amended paragraph:

FIG. 6D is a flow diagram of a specific embodiment of a process 670 for deriving sample timing with reduced jitter for a received signal instance. Initially, a determination is made whether or not the pilot SINR for the signal instance is greater than a particular threshold (step 672). If the answer is no, then the process returns to step 672. Otherwise, if the pilot SINR is greater than the threshold, then the delay lock loop enters the enhanced mode and two slave pilot processors are assigned to the signal instance (step 674). The modified time offsets for these slave pilot processors are then determined, and the pilot SINRs of the slave pilot processors are also initialized (step 676). Because measurement noise could cause the pilot SINR of a slave pilot processor to be momentarily larger than that of the master pilot processor, which may possibly lead to DLL jitter, the pilot SINRs of the slave pilot processors may be set equal to the pilot SINR of the master pilot processor minus a particular amount.

On page 19, please replace paragraph [1019] with the following amended paragraph:

The loop filter of the master pilot processor is updated for each loop update period (e.g., every half-slot) based on the error metric derived by the early/late discriminator of the master pilot processor (step 682). The output of the loop filter is monitored for jitter. If the loop filter output implies retention of the current time offset, t_{adj}, (step 684), then no additional processing is required and the process returns to step 682. Otherwise, if the loop filter output implies a change in the time offset, t_{adj}, to a new value that is either +1 or -1 chipx8 unit away from the

prior value (step 684), then the slave pilot processor corresponding to the new time offset is identified (step 686). The pilot SINR of the master pilot processor is then compared against the pilot SINR of the identified slave pilot processor, which was previously assigned with the new time offset (step 688).